Silicon Neuron dedicated to Memristive Spiking Neural Networks

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***Abstract*—Since memristor came out in 2008, neuromorphic designers investigated the possibility of using memristors as plastic synapses due to their intrinsic properties of plasticity and weight storage. In this paper we will present a silicon neuron compatible with memristive synapses in order to build analog neural network. This neuron mainly includes current conveyor (CCII) for driving memristor as excitatory or inhibitory synapses and spike generator whose waveform is dedicated to synaptic plasticity algorithm based on Spike Timing Dependent Plasticity (STDP). This silicon neuron has been fabricated, characterized and finally connected with a ferroelectric memristor to validate the synaptic weight updating principle.**

I. Introduction

In 1971 L. Chua predicted the existence of memristor [1], but it is only since 2008 and the response of the HP team [2] to the theorist, that memristive components have renewed interest. So far, this element has the capability to change resistance according to the current flowing through it and to memorize the modification. This intrinsic property can be used for different applications: memory [3], logic [4] and neuromorphic systems.

In the field of neuromorphic engineering, analog or mixed mode hardware implementations have been proposed [5] to build bio-inspired systems. Analog implementation takes advantage from the locally analog and parallel nature of the computations. Those systems are based on spiking silicon neurons in real time [6]. The designers use biological principles, taking various approximations of nature, with the view to build more efficient systems. However, the spiking neural networks (SNN) need to store the synaptic weights which will be changed during the learning period.

Therefore, memristors constitute an ideal and very timely alternative implementation for synapses of hardware SNNs. Memristors combine the advantages of having a nano-size to build larger SNN, being a non-volatile memory to reduce power consumption and having an intrinsic plasticity to update synaptic weight. Hardware SNNs with an architecture composed of analog circuitry coupled with the aforementioned memristors open the possibility to build high-performance accelerators able to tackle the large computational tasks.

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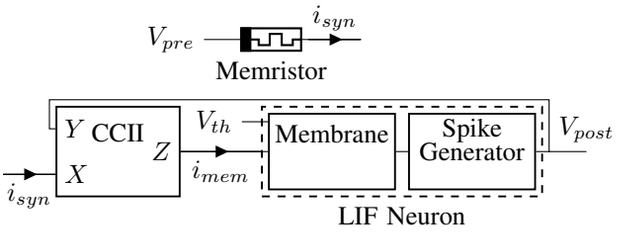


Fig. 1. Silicon neuron dedicated to excitatory or inhibitory memristive synapses.

In MHANN project, we focus on "ferroelectric memristor" [7]. The advantage of this technology is a purely electronic switching promissing large speed and high reliability. As shown in [8], with memristors it is possible to have access to different resistance values. Moreover their resistances are high (between $1M\Omega$ and $1G\Omega$) and their voltage thresholds are around $|2V|$. This component has the required characteristics to be used with CMOS technologies.

In SNN, plasticity of synapse is mandatory for learning mechanism. The spike-timing dependent plasticity (STDP) is commonly used. STDP depends on relative timing of pre- and post-synaptic spikes. To use a memristor as a synapse we have to translate this relative timing into voltage difference. In [9], we have proposed a solution to gather memristive synapses and spiking neurons. The purpose of this paper is to present measurements which will validate our concept. The design of such silicon neuron is presented in Sec. II. Measurements of some building test blocks are detailed in Sec. III. In Sec. IV, we connect one ferroelectric memristor to our chip to validate the synaptic weight update.

II. Circuit

Our silicon neuron is composed of a leaky integrate and fire neuron (LIF neuron) and a second generation current conveyor (CCII) as shown in Fig. 1. This arrangement permits us to insert a memristive component before the neuron.

A. LIF Neuron and Spike generator

As it is proposed in [10] or in [11], LIF neuron is separated in two blocks. The membrane block includes in parallel one

$1.6M\Omega$ resistance for leaky effect, one $700fF$ membrane capacitance to sum inputs contributions i_{mem} and one switch to reset the capacitor. When the membrane voltage reaches threshold potential V_{th}, comparator triggers the spike generator block: an action potential is also output.

Theoretical studies in [10], point out importance of spike shape for learning mechanism of memristive spiking neural networks. Indeed it is the spikes that make the translation of voltage-time. The shape of the spike directly influences the resulting STDP. We chose to work with STDP that gives potentiation of synaptic weight for $\Delta t > 0$, and a depreciation for $\Delta t < 0$, with $\Delta t = t_{post} - t_{pre}$, where t_{post} being trigger time of post-synaptic spike and t_{pre} being trigger time of pre-synaptic spike.

We chose spike form as illustrated in Fig. 2. It is generated by the second block of LIF neuron called spike generator. It is based on the *Axon-Hillock* circuit [12], which allows us to control timing and amplitudes parameters t_{spk}, t_{LTx}, $A_{offset_{max}}$ and $A_{offset_{min}}$. During t_{spk} pulse, a transmission gate switches the output to A_{spk} constant voltage adjustable outside the chip contrary to other spike settings.

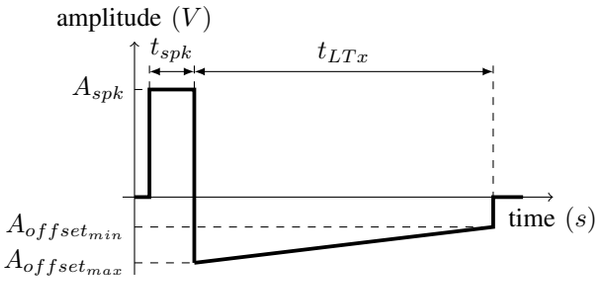


Fig. 2. Shape of the spike.

B. CCII

The current conveyor provides impedance matching between synapse and neuron. The voltage at X (one memristor terminal) follows that applied to Y (post-synaptic voltage). The current supplied to X (synaptic current) is convoyed to the output terminal Z (LIF neuron input) where it is supplied with either positive polarity (excitatory synapse) or negative polarity (inhibitory synapse). On the other words, the memristor voltage is $V_{pre} - V_{post}$. Then the memristor current i_{syn} is always injected into CCII and i_{mem} is equal to $+i_{syn}$ or $-i_{syn}$ following the excitatory (using an CCII+) or inhibitory (using an CCII-) type of the synapse respectively.

The CCII design is inspired from the description given in [13] and has been adapted to input voltage range ($0.85V$ to $4V$) and bandwidth required for minimum $100ns$ pulse width transmission.

C. Fabrication

We have designed a chip called SpANNWiTA (*Spiking Analog Neural Network Winner Take All*) using 6ML $0.18\mu m$ CMOS technology from Austriamicrosystems under Cadence

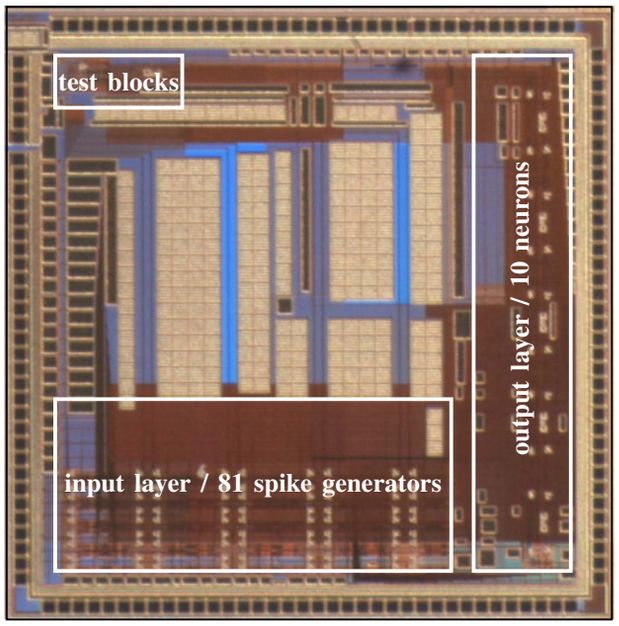


Fig. 3. Microphotography of SpANNWiTA.

Analog Design Environment using Spectre simulator. The die shown in Fig. 3 has an area of $3 \times 3mm^2$ and 142 pads ; it has been packaged using PGA 144. The chip includes the two layers of a neural network (81 x 10, all to all connected using external crossbar of memristors), and several test blocks for characterization. All the measurements that are presented in the next section have been done using these blocks.

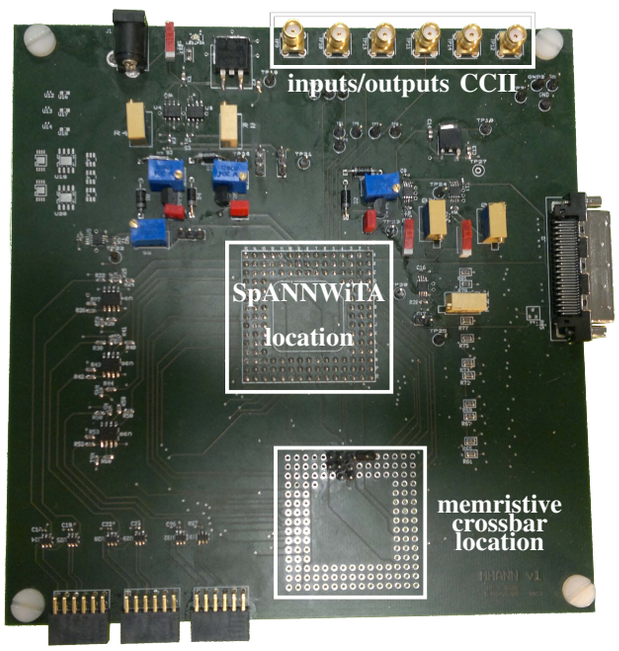


Fig. 4. Photography of the measurement board.

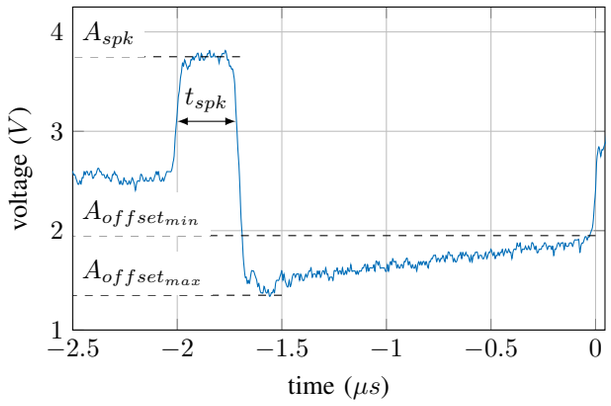
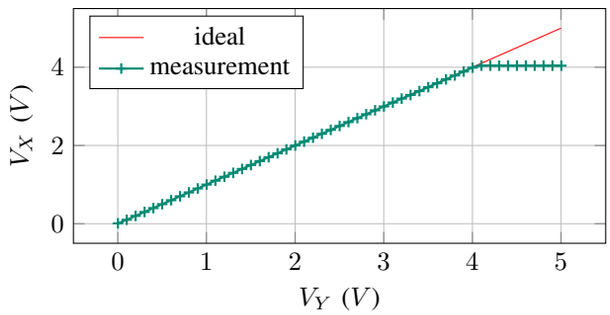


Fig. 5. Measurement of the spike generator output.

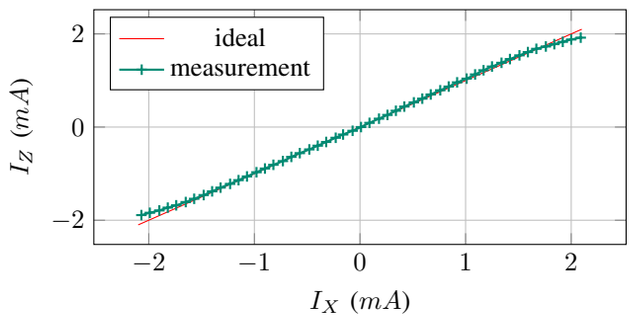
III. Circuit Measurements

A. Measurement environment

We have designed a specific board as shown in Fig. 4 dedicated to chip characterization and future network management. For routing convenience, the chip SpANNWiTA is plugged on the bottom side. This board provides a $5V$ power supply with the mid point at $2.5V$ and different biasing current sources, $10\mu A$ for each neuron and $30\mu A$ for each current conveyor. To perform the following measurements we use Agilent Mixed Signal Oscilloscope, Waveform Generator and Keithley Picoammeter.

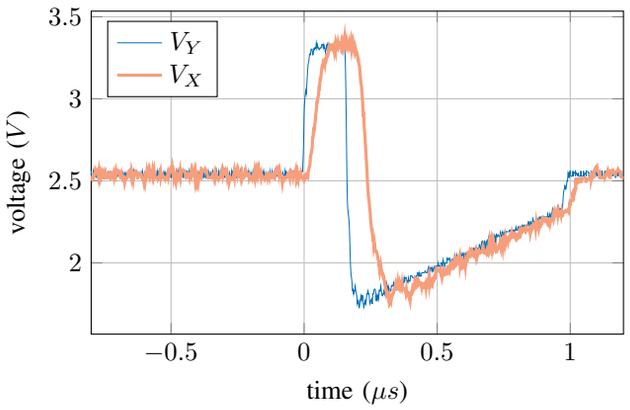


(a) Voltage follower test in DC mode: copy of V_Y on V_X.

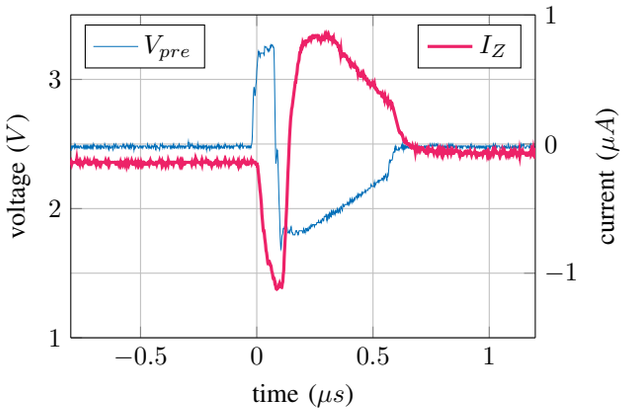


(b) Current follower test in DC mode: copy of I_X on I_Z.

Fig. 6. Static CCII+ characterization in terms of voltage (a) and current (b).



(a) Voltage copy of an action potential applied at Y CCII+ input to X input.



(b) I_Z CCII+ output current when an action potential is applied at V_{pre} with a resistor of $1M\Omega$ at X simulating a memristor.

Fig. 7. Dynamic CCII+ characterization in terms of voltage and current.

B. Spike generator characterization

For testing the pulse generator we set the voltage A_{spk} to $3.75V$. The measure pulse shown in Fig. 5 as the same waveform than one of Fig. 2. $A_{offset_{max}}$ and $A_{offset_{min}}$ are equal to the wished voltage value that is important for plasticity rules [10]. However t_{spk} lasts three times more than expected. As described in [8], the memristor plasticity depends on the applied voltage and the application time. Thanks to A_{spk} wich is a tunable parameter, we will overtake that drawback.

C. CCII characterization

We have started by testing the DC behavior of the current conveyor. We got the same results for both CCII+ and CCII-. In Fig. 6(a), the V_X voltage follows the slow voltage ramp applied to Y input within a range of $0V$ to $4V$. For CCII+, the output current I_Z follows the input current I_X generated by a ramp voltage applied on V_{pre} input and through $1k\Omega$ resistor at memristor location of Fig. 1.

For characterizing the dynamic behavior, a waveform generator applies a spike waveform on Y input that is copied on X input with a little delay, as shown in Fig. 7(a). In another test

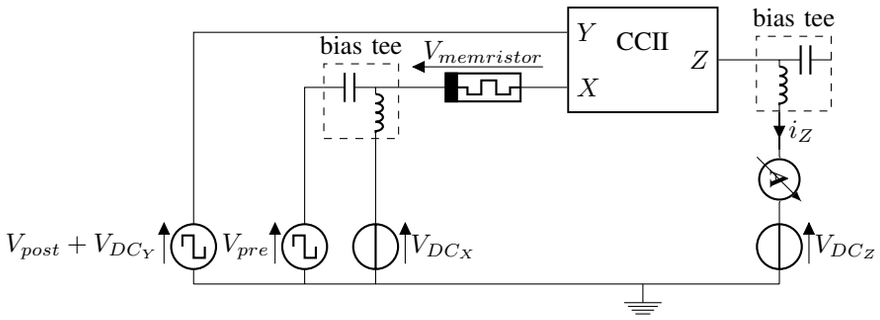


Fig. 8. Memristor & CCII measurement platform.

illustrated in Fig. 7(b), we have fixed the V_Y input voltage to $2.5V$ and the output current I_Z is the copy of the I_X current generated by a spike waveform applied on V_{pre} input through a $1M\Omega$ resistor.

IV. Memristive synapse

Due to high resistance value of memristor, currents through this component are weak. The unique solution for measurement is to use a picoammeter. Using SMA cable, we have connected a ferroelectric BFO memristor [14] to CCII input. The measurement platform is shown in Fig. 8. The bias tee connected to memristor avoids memristor value change due to artefacts. The second bias tee rejected AC current that allows DC accurate measurements with the picoammeter. Potential V_{DC_X}, V_{DC_Y} and V_{DC_Z} are set to $2.5V$. Two waveform generators are used to deliver V_{pre} and V_{post} neuron spikes with a controlled delay Δt. Finally, during the reading phase, we adjust V_{DC_X} to $2.7V$, thus $0.2V$ potential difference is applied to the memristor. Then we measure CCII output current I_Z, image of the memristor value, with a picoammeter.

Before applying the first difference of spike, we measure a current i_Z equal to $0.20\mu A$. We can deduce $R_{memristor} \approx 1M\Omega$. Then a spike is generated at V_{post} and $200ns$ after, an other spike is generated at V_{pre}. We read $i_Z = 0.03\mu A$ so $R_{memristor} \approx 6.66M\Omega$. Memristor resistance value has increased as expected ($\Delta t = t_{post} - t_{pre} < 0$, synaptic weight decreases and memristor resistance increases). After, two pairs of spike are generated with $\Delta t = 100ns$, we measure $i_Z = 0.09\mu A$ ($R_{memristor} \approx 2.22M\Omega$) then $i_Z = 0.19\mu A$ ($R_{memristor} \approx 1.05M\Omega$). As previously, the memristor resistance has changed. But this time Δt was positive, so synaptic weight had to increase, that means resistance had to decrease, as we observed.

The memristor resistance is modified with potential spike difference. So the current conveyor is working as predicted in simulation [9].

V. Conclusion

In this paper, we have characterized the building blocks of our silicon neuron dedicated to the design of memristive spiking neural networks. The measurements validate our design. Then by connecting real BFO memristor with CCII we have demonstrated it is possible to modify memristor resistance *ie* synaptic weight, in real time thanks to spike delay. We proved our concept is efficient for the design of memristive neural networks.

The next step will be to connect the silicon neurons shown Fig. 3 with a crossbar of memristors.

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